REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 4-6, 8, 9, 13, and 15-20 are presently active in this case. Claims 1, 5, 9, and 13 have been amended by way of the present amendment.

First, Applicant acknowledge with appreciation the courtesy of an interview granted to Applicant's attorney on December 8, 2003 at which time the subject invention was explained in light of Applicant's disclosure and the outstanding issues were discussed. Proposed changes to overcome the 35 U.S.C. § 112, second paragraph, rejections were discussed and agreed upon.

In the outstanding Office Action, the title of the invention was objected to for not being descriptive; the abstract of the disclosure was objected to for being unclear; formal drawings were required; the specification was objected to for including minor errors; Claim 5 was objected to for being unclear; Claims 1, 4, 9, 13, and 15-20 were rejected under 35 U.S.C. § 112, second paragraph, for being indefinite; Claims 9 and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al; Claims 1, 4, 15, 18, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,603,001 to Sukegawa et al. in view of Lee et al.; Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sukegawa et al. and Lee et al.; and Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sukegawa et al. in view of Lee et al. and Bruce et al.

In response to the objection to the title, Applicant has amended the title to read "Nonvolatile Semiconductor Memory Having Plural Memory Circuits Selectively Controlled by a Master Chip Enable Terminal or an Input Command and Outputting a Pass/Fail Result". No further objection on this basis is therefore anticipated.

In response to the objection to the abstract, the abstract has been rewritten to change "Electronically" to --Electrically--. No further objection to the abstract is therefore anticipated.

In response to the requirement to file corrected drawings, Applicant has submitted herewith 3 replacement sheets of drawings.

In response to the objections to the specification, Applicant has amended the specification as recommended by the Examiner. Applicant would like to note the following. First, Applicant would like to point out that the recitation of "these signals" on page 5, line 2 should be changed to read "enable signals." As the Official Action correctly points out, enable signals are input to the control circuit. Second, regarding the objection to the recitation "a little control continues to enter each of the EEPROM circuits" on page 7, lines 35 and 36 of the original specification, Applicant has amended that recitation to recite that "it is seldom that each EEPROM circuit is controlled continuously". Finally, regarding the objection to the passage beginning on page 9, line 11, Applicant point out that the correct description should be that "each of the EEPROM circuits 2 does not include controllers of command, address, and data." No new matter has been added.

In response to the objection of Claim 5, Claim 5 has been rewritten as recommended in the Office Action. No further objection on this basis is therefore anticipated.

In response to the rejection of Claims 1, 4, 9, 13, and 15-20 under 35 U.S.C. § 112, second paragraph, those claims have been amended consistent with the claim changes discussed during the interview. No further rejection under 35 U.S.C. § 112, second paragraph, is therefore anticipated. However, if any issues remain, the undersigned hereby invites the Examiner to request a personal or telephonic interview.

Claims 1 and 5 have been rewritten to clarify that the memory circuits are provided on a single memory chip, that each memory circuit has a respective chip enabled terminal, and

that a master chip enable terminal is provided for controlling the activity and inactivity of the memory chip as a whole. Consequently, as discussed during the interview, Applicant respectfully submit that the applied prior art does not anticipate or render obvious the subject matter defined by Claims 1 and 5 when considered alone or in combination with one another.

Claim 9 has been amended to clarify that the at least one data buffer stage stores writing data corresponding to an address and that a pass/fail result of each of the writing operations is output to each of the memory circuits and accumulated in the corresponding at least one data buffer stage. No new matter has been added. See page 10, lines 18 – page 11, line 3 of the specification.

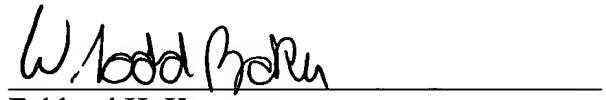
Lastly, Claim 13 has been amended to clarify that the electrically rewritable nonvolatile semiconductor has a mode whereby each of the plurality of memory circuits determines whether data is able to be inputted to said corresponding at least one data buffer stage by referring to the memory circuit's corresponding pass/fail results, and a mode in which each of the plurality of memory circuits determines whether data is able to be input to the corresponding at least one data buffer stage without referring to the corresponding pass/fail results.

Applicant respectfully submit that the applied prior art does not anticipate or render obvious the subject matter defined by Claims 9 and 13, respectively.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

W. Todd Baker
Registration No. 45,265

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

I:\ATTY\WTB\0039\200714\AMENDMENT 23 FEB 2004.DOC